ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes a cell block composed of several series-connected units having a ferroelectric capacitor and a cell transistor parallel-connected to the ferroelectric capacitor and a select transistor connected to an end of the cell block. Mutually separated first impurity diffusion layers are formed on the surface of the semiconductor substrate along a first direction, and have a first area. A second impurity diffusion layer is formed on the surface of the semiconductor substrate separated from the end first impurity diffusion layer, and has a second area. A first gate electrode is provided on the semiconductor substrate between the first impurity diffusion layers along a second direction. A second gate electrode is provided on the semiconductor substrate between the end first impurity diffusion layer and the second impurity diffusion layer along a second direction. A contact electrically connects a bit line and the second impurity diffusion layer.